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REVIEW: ELECTRICAL PROPERTIES OF SILICON CARBIDE-BASED COMPOSITE MATERIALS

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Silicon carbide (SiC) is a wide-bandgap semiconductor that is widely used in power electronics, automotive industries, and aerospace applications due to its high thermal conductivity and breakdown field. This review examines both the fundamental physics and the practical applications of SiC. We analyze its major crystal structures (polytypes), specifically 4H-SiC, 6H-SiC, and 3C-SiC, and discuss how these structures affect electrical performance. The paper also covers new developments in SiC functional ceramics, metal-matrix nanocomposites, and quantum defects used for quantum information science. By analyzing research literature from 2006 to 2026, we show how the industry transitioned from basic crystal growth to 8-inch wafer manufacturing and automated defect classification using neural networks. Finally, this review discusses the main technical problems that still limit SiC devices, such as high interface trap density (D_{it}), high contact resistance in p-type doping, and bias temperature instability (BTI). By comparing theoretical material properties with real device performance, this paper identifies key research priorities for the next generation of semiconductor technology.

Keywords: SiC, wide bandgap semiconductors, electronic transport, interface traps, electrical properties, nanocomposites, quantum defect engineering, dielectric loss mechanisms, high-temperature electronics

INTRODUCTION

Silicon carbide (SiC) is one of the most important wide-bandgap (WBG) semiconductors today, driving electrification across automotive, renewable energy, and aerospace industries. Its key strengths include a high critical breakdown field (~ 3.0 MV/cm), strong thermal conductivity ($3.7 \dots 4.9$ W/cm $\cdot$ K), and stable operation up to 500°C [1-5]. Modern growth techniques like Physical Vapor Transport (PVT) and High-Temperature Chemical Vapor Deposition (HT-CVD) now enable 8-inch (200 mm) wafers, making SiC cost-competitive with GaN and Ga_2O_3 for power devices in the $1.2 \dots 10$ kV range [5-8]. A defining feature of SiC is its polytypism over 250 crystal forms exist depending on atomic layer stacking, which directly affects band structure, carrier mobility, and polarization [1, 4, 5, 9]. Among these, 4H-SiC is preferred for vertical power MOSFETs due to its uniform electron mobility of ~ 900 cm ^{2} /V $\cdot$ s [1, 5]. By contrast, 6H-SiC exhibits problematic mobility anisotropy [9, 10], while 3C-SiC suffers from stacking faults caused by a $\sim 20\%$ lattice mismatch on silicon substrates [11-14]. Beyond bulk devices, SiC research spans a wide range of forms. Porous and sintered SiC ceramics are explored for thermoelectric conversion, filtration, and EMI shielding [15-17]. Cu-SiC nanocomposites balance conductivity and low thermal expansion for contacts and heat sinks [18, 19]. SiC nanowires and nanotubes are studied for miniature transistors and gas sensors [20, 21]. Point defects such as silicon vacancies (V_{Si}) and divacancies ($V_{\text{C}}V_{\text{Si}}$) serve as room-temperature qubits and single-photon sources for quantum computing [11, 22]. SiC-

boron nitride nanosheet (SiC-BNNS) composites and core-shell nanofibers are also embedded in polymers for microwave absorption and radar cross-section reduction [23-25]. Research from 2006 to 2026 shows clear growth in the field. Early work focused on crystal growth and defect reduction; between 2012–2020, the focus moved to process optimization, contact engineering, and 150 mm substrates [26-28]. Since 2020, new directions have emerged including high-k gate dielectrics [29, 30], post-oxidation annealing [31-33], AI-based defect classification [34-38], and the commercial shift to 8-inch wafers [8]. Despite this progress, key challenges remain: high interface trap density D_{it} at the SiC/SiO $_2$ interface, poor p-type contact resistance, and bias temperature instability (BTI) under prolonged stress [39-42]. This review critically examines transport mechanisms, doping dynamics, and radiation hardness data to identify priorities for future research [39-42].

To support practical device design comparisons, the key physical and transport parameters of the most relevant SiC polytypes are summarized in Table 1.

Table 1. Physical and electronic properties of major SiC polytypes compared to Silicon.

Property	3C-SiC (Cubic)	4H-SiC (Hexagonal)	6H-SiC (Hexagonal)	Si (Reference)
Stacking Sequence	ABC...	ABCB...	ABCACB...	Diamond
Hexagonality (h, %)	0	50	33.3	0
Energy Bandgap (Eg, eV at 300 K)	2.36	3.23	3.05	1.12

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Property	3C-SiC (Cubic)	4H-SiC (Hexagonal)	6H-SiC (Hexagonal)	Si (Reference)
Critical Breakdown Field (E_c , MV/cm)	1.2	3.0	2.4	0.3
Electron Mobility	900	900 (lto c), 900 ($\perp$ to c)	60 (lto c), 400 ($\perp$ to c)	1450
Saturated Electron Velocity	2.5	2.0	2.0	1.0
Thermal Conductivity	4.9	4.9	4.9	1.5

MEASUREMENTS AND INFLUENCING FACTORS

1. Electronic Transport in SiC Polytypes: From Intrinsic Properties to Device-Relevant Parameters

Band Structure Limits and Polytype-Dependent Mobility

Electron movement in SiC is fundamentally governed by its polytypism changes in atomic layer stacking directly affect the band structure, carrier effective mass, and scattering behavior [1, 7, 9]. Of more than 250 known crystal forms, three matter most for power electronics: 4H-SiC, 6H-SiC, and 3C-SiC [1, 4, 11].

4H-SiC dominates high-voltage vertical devices thanks to its symmetric conduction band minima and low directional variation in electron effective mass [1, 7, 9], giving it a bulk electron mobility (μ_n) of $\sim 900\text{--}1000\text{ cm}^2/\text{V}\cdot\text{s}$ at room temperature [1, 9]. 6H-SiC, by contrast, suffers from strong carrier scattering due to its ABCACB stacking sequence, weakening its transport performance [9]. While 3C-SiC theoretically offers the highest bulk mobility of the three, its growth on silicon substrates produces thermal mismatch-induced stacking faults and microtwins that block transport paths and reduce device yields in practice [11, 43].

Scattering Mechanisms and High-Temperature Transport Stability

SiC's wide bandgap suppresses intrinsic carrier generation, enabling reliable device operation above 500°C – a major advantage over silicon [1, 27]. At such temperatures, transport remains controlled by intentional dopants rather than thermally generated carriers, underpinning SiC's high-temperature stability [2, 27, 44].

In real devices, carrier drift is shaped by competing scattering mechanisms: acoustic and optical phonon interactions, ionized impurity scattering, and defect trapping [7, 39, 45]. At low fields, impurity scattering limits mobility; at high fields, optical phonon emission saturates carrier velocity. Balancing these effects through careful doping profile optimization is essential to minimize conduction losses while maintaining breakdown voltage.

Crystallographic Defects, Anisotropy, and Bipolar Reliability

The main reason SiC layers fall short of theoretical transport limits is the presence of extended crystallographic defects – basal plane dislocations (BPDs), threading screw dislocations (TSDs), threading edge dislocations (TEDs), and micropipes [41, 45, 46]. While PVT process improvements have eliminated micropipes from modern 200 mm wafers [4], smaller dislocations remain problematic. They act as non-radiative recombination centers, shortening carrier lifetimes and increasing leakage current. In bipolar devices under sustained forward current, BPDs migrate and decompose into Shockley stacking faults, causing forward voltage drop (ΔV_f) drift and long-term reliability loss [41, 47–49]. This has shifted modern SiC research increasingly toward defect-driven degradation management rather than fundamental transport physics [39, 42]. Transport anisotropy adds further complexity. In 4H-SiC, electron mobility differs

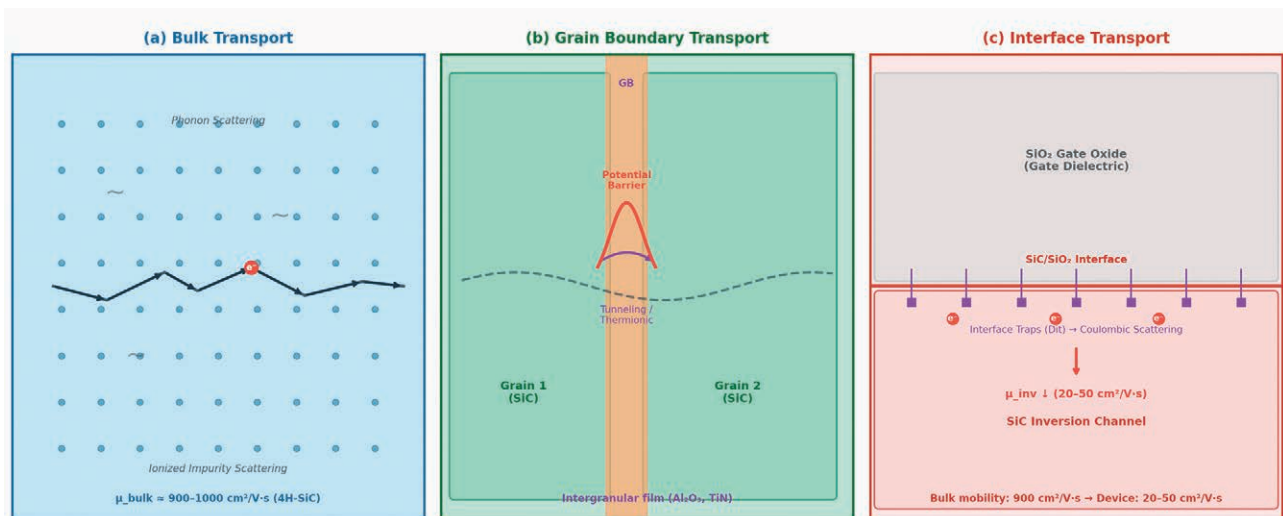


Figure 1. Electronic transport mechanisms in SiC: (a) bulk phonon and impurity scattering, (b) grain-boundary potential barriers and tunneling, (c) interface trap density (D_{it}) Coulombic scattering reducing inversion-channel mobility.

between directions parallel and perpendicular to the c-axis (0001) [1, 9], which becomes critical in trench-gate MOSFETs where current flows through non-standard planes such as the (1120) a-plane or (1100) m-plane [50]. Mobility varies across these surfaces due to roughness, atomic packing, and dangling bond differences, making precise crystallographic alignment during wafer cutting and etching essential [41, 50].

Interfacial Bottlenecks and Device Translation

Bulk transport parameters only set the theoretical performance ceiling. In practice, actual device efficiency is limited by near-surface transport, surface roughness scattering, and contact resistance [7, 39, 40]. A large gap exists between bulk mobility and the inversion layer channel mobility (μ_{inv}) measured in real devices, primarily because high interface trap density (D_{it}) near the conduction band edge immobilizes carriers and causes strong Coulombic scattering [39, 42].

Reliability under repeated thermal and electrical stress is equally challenging. Microscopic defect propagation and interface degradation under high-field conditions directly cause threshold voltage shifts and bias temperature instability (BTI) [51]. Bulk transport analysis alone is therefore insufficient to predict real device behavior. Fully realizing SiC's efficiency advantages requires combining bulk defect reduction with advanced passivation at both the interface and contact level [39, 41, 51].

2. POROSITY, DOPING, AND SINTERING EFFECTS

Porosity and Structural Regulation of Resistivity

Controlling the electrical resistivity of SiC-based ceramics is critical for designing heating elements, power hardware, and electromagnetic shielding components. By adjusting the doping profile and the microstructure of the material, resistivity can be tuned across a very wide range from fully insulating to highly conductive behavior [15]. Nitrogen is the main donor impurity, occupying carbon lattice sites to create n-type conductivity. However, in porous SiC matrices, the overall transport efficiency is significantly reduced by grain boundary scattering and the presence of secondary phases [15, 16, 52].

This reduction in conductivity is not a simple linear effect. As the volume fraction of pores increases, conductivity drops exponentially. This behavior follows percolation theory rather than a straightforward volumetric relationship [17]. The reason for this steep drop is a combination of two factors: the effective cross-sectional area available for conduction shrinks dramatically, and the path that current must follow becomes increasingly tortuous [17]. Importantly, detailed comparative analysis shows that the total amount of porosity is often less important than the shape and connectivity of the pores. The degree to which the SiC skeleton remains interconnected, and the ratio of open pores to closed pores, have a much greater influence on the final resistivity than the total pore volume percentage alone [15, 17].

Table 2. Processing and microstructural factors influencing the electrical properties of SiC ceramics

Processing Parameter / Feature	Applied Range / Condition	Impact on Electrical Conductivity / Resistivity	Underlying Physical Mechanism
Porosity Scaling	32% to 54% volume fraction	Exponential non-linear drop in conductivity	Restriction of effective conduction cross-section; increased path tortuosity matching percolation limits.
Liquid-Phase Sintering (LPS)	Oxide additives (Al ₂ O ₃)	Elevated bulk resistivity	Formation of an amorphous, insulating intergranular film establishing an electrostatic potential barrier.
Conductive Phase Additives	Transition metal nitrides/carbides (TiN, ZrN)	Suppression of resistivity down to $\sim 10^{-2} \Omega \text{ cm}$	Formation of conductive pathways/bridges across adjacent SiC grain junctions.
P-type Doping (Aluminum)	Acceptor activation ($\sim 90...250 \text{ meV}$)	High, non-linear temperature dependence of resistance	Incomplete carrier ionization at room temperature; requires heavy near-interface doping $> 10^{19} \text{ cm}^{-3}$
Thermal Budget (Ceramic Composites)	Annealing at $\sim 1600^\circ\text{C}$	Irreversible surge in macro-resistivity	Thermal degradation of conductive secondary phases segregated at the grain boundaries.

Sintering Dynamics and Phase Engineering

The high-temperature process used to consolidate SiC powders into dense ceramics introduces important changes in electrical behavior. When Liquid-Phase Sintering (LPS) is performed using oxide additives such as Al₂O₃, an amorphous and electrically insulating secondary layer forms at the boundaries between grains [15, 16]. This intergranular film creates an electrostatic energy barrier that blocks electron tunneling between grains and raises the overall bulk resistivity compared to solid-state sintering alternatives. To overcome this barrier, recent research has introduced conductive transition metal nitrides or carbides – such as TiN or ZrN – as secondary additives [16]. These materials form conductive bridges between neighboring SiC grains, and can bring resistivity down to around $10^{-2} \Omega \cdot \text{cm}$ even in highly porous structures [16].

P-type Doping Challenges and Ohmic Junctions

Achieving efficient p-type conductivity in SiC through aluminum (Al) substitution remains one of the most difficult problems in the field. This challenge directly limits the current-carrying capability and forward voltage stability of kilovolt-class junction barrier Schottky (JBS) diodes [53]. During crystal growth, this requires careful control of the carbon-to-silicon transport ratio in top-seeded solution growth processes, in order to suppress the formation of defects [54]. The core problem is a fundamental physical one: aluminum acceptors in SiC have a high activation energy of approximately 190 to 250 meV, which means they cannot fully ionize at room temperature [40]. As a result, while n-type SiC devices show stable

and predictable carrier behavior, p-type devices exhibit a strong and non-linear dependence on temperature. To overcome this ionization barrier and form high-quality Ohmic contacts, very heavy doping near the interface (above 10^{19} cm^{-3}) is required, along with high-temperature annealing to enable field-emission tunneling. Using this approach, researchers have achieved a low specific contact resistance (R_c) in the range of $10^{-5} \Omega \cdot \text{cm}^2$ [40].

Thermal Stability and Application Priorities

The research literature reveals two very different approaches to thermal treatment, depending on the type of SiC material being used. For single-crystal materials such as 6H-SiC, high-temperature annealing at 1600°C is commonly applied to remove compensating point defects and stabilize the semi-insulating baseline behavior [50]. However, applying the same thermal conditions to SiC ceramic composites causes the opposite effect – it degrades the conductive secondary phases located at the grain boundaries, leading to an irreversible and large increase in bulk resistivity [15, 16]. This contrast points to a clear division in engineering goals. Single-crystal power electronics require uniform spatial distribution of dopants throughout the material. Functional ceramic structures, such as heatable filters or EMI absorbers, instead require precise control of grain boundary chemistry and pore geometry in order to maintain a stable balance between electrical performance and thermal processing limits [15, 16, 50].

3. INTERFACE STATES AND SiC/SiO₂ PROPERTIES (MOSFET STRUCTURES)

Interfacial Traps and Chemical Passivation Trade-offs

The performance of commercial SiC power MOSFETs is heavily limited by the electronic quality of the thermal SiC/SiO₂ interface, which acts as a critical bottleneck for carrier transport [5, 55]. Near the conduction band edge, the interface trap density (D_{it}) in SiC devices regularly exceeds the equivalent value at the classic Si/SiO₂ interface by roughly two orders of magnitude [39]. These interface traps arise primarily from localized carbon clusters, defects in the oxide near the interface, and stress introduced during thermal processing. They cause intense Coulombic scattering that pulls the inversion layer channel mobility (μ_{inv}) far below the theoretical bulk mobility values [7, 39, 56].

Reducing this problem requires targeted interface engineering strategies. Examples include CO₂ post-deposition annealing of sputtered oxides, or replacing the traditional gate dielectric with alternative materials such as Si₃N₄. However, each of these approaches involves trade-offs between improving mobility, maintaining threshold voltage (V_{th}) stability, and controlling defect density [57, 58]. The specific effects of different passivation methods on near-surface transport properties are summarized in Table 3.

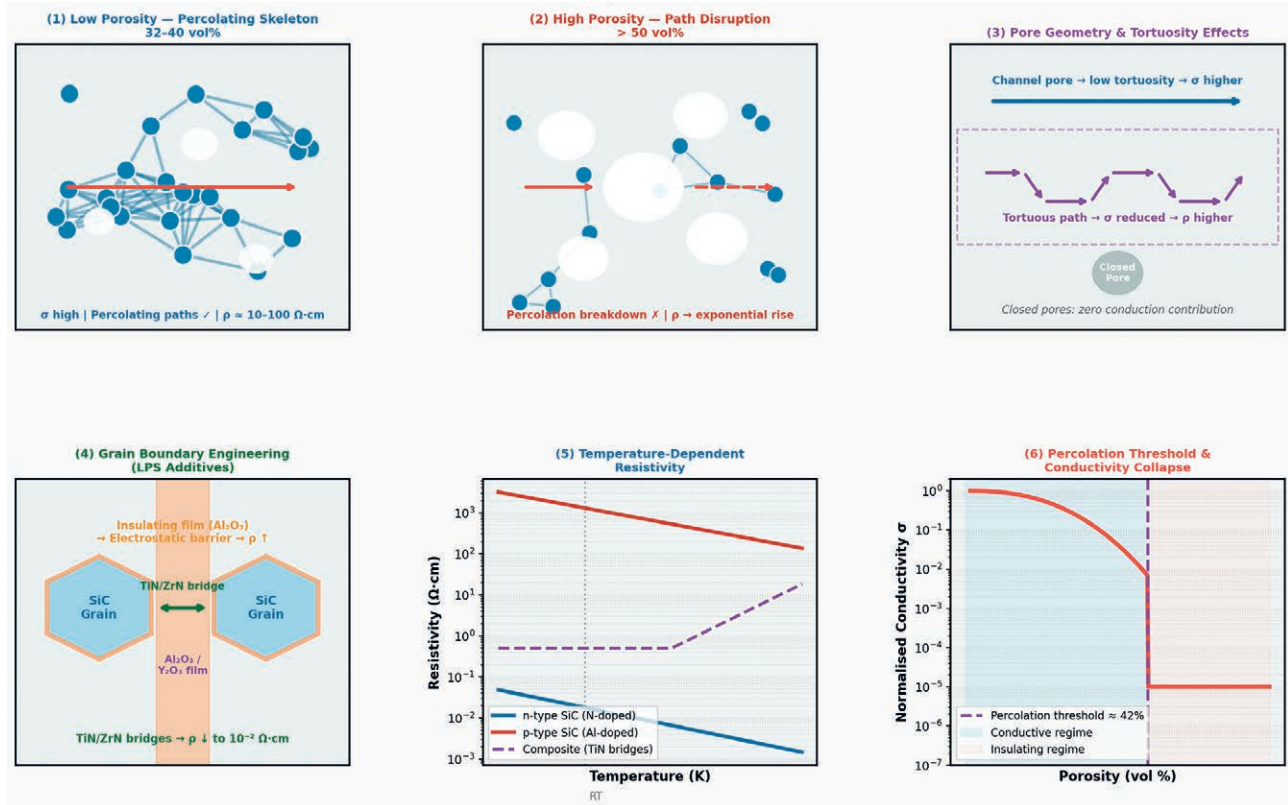


Figure 2. Microstructural and electrical effects in porous SiC ceramics: (1-2) percolation regimes, (3) pore geometry and tortuosity, (4) grain-boundary engineering, (5) temperature-dependent resistivity, (6) percolation threshold and conductivity collapse

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Table 3. Comparative evaluation of interface passivation techniques on 4H-SiC MOSFET performance

Passivation Strategy / Condition	Interface Trap Density D_{it} ($\text{cm}^{-2}\cdot\text{eV}^{-1}$)	Inversion Layer Channel Mobility μ_{inv} ($\text{cm}^2/\text{V}\cdot\text{s}$)	Threshold Voltage (V_{th}) Stability	Dominant Reliability Limitation
Unpassivated Baseline	1012...1013	20...30	Poor	Severe Coulombic scattering; high near-interface trap capture.
Standard Nitrogen (NO Annealing)	Moderate reduction	35...40	Stable	Insufficient trap screening near the conduction band edge.
Phosphorus / Boron Passivation	Significant reduction	80...100	Unstable	Accelerated V_{th} drift; high vulnerability to bias temperature instability (BTI).
Advanced High-k Dielectrics	Variable	Highly structural dependent	Device specific	

Electrostatic Scaling, Strain, and Reliability Barriers

Apart from chemical approaches, near-surface carrier transport is also strongly affected by mechanical and structural design choices. For example, applying a uniaxial tensile strain to the material changes the curvature of the conduction band and reduces the electron effective mass. This results in a measurable boost in drain current of more than 10% [50].

From an architectural standpoint, vertical trench MOSFET layouts (UMOSFETs) can achieve higher current densities than planar designs (DMOSFETs). However, they also create intense localized electric field crowding at the trench corners, which reduces the net breakdown voltage by approximately 20% [50].

Long-term device reliability is also compromised by dynamic charge trapping effects. Defects located very close to the interface – often called «border traps» – along with slow-moving carbon defects, act as charge-trapping centers. Under sustained high-temperature operation at 175°C, these traps cause significant threshold voltage (V_{th}) shifts exceeding 0.5V [7, 42]. At the nanoscale level, switching to gate-all-around (GAA) nanowire MOSFET geometries (NW-FETs) offers excellent electrostatic control over the channel. This effectively eliminates short-channel effects and produces a high current switching ratio (I_{on}/I_{off}) greater than 10^6 , which is useful for specialized high-temperature sensor applications [20]. However, these nanostructures are inherently limited by very small absolute current levels in the microampere range. This

stands in sharp contrast to the kiloampere-level currents required by heavy-duty power modules [20, 39].

4. ELECTRICAL PROPERTIES OF SiC-BASED NANOCOMPOSITES AND FILMS

Metal-Matrix Nanocomposites and Interfacial Transport

Designing SiC-reinforced metal-matrix composites (MMCs) requires finding the right balance between structural and thermal stability on one hand, and electrical conductivity on the other. When semi-insulating SiC particles are added to a highly conductive copper (Cu) matrix, the overall electrical conductivity of the composite decreases. This happens because the SiC-metal junctions scatter charge carriers, and because small residual pores remain in the microstructure [18]. However, research data shows that the shape and size of the SiC filler particles can help reduce this conductivity loss. Using nano-scale SiC particles instead of micro-scale particles helps maintain higher electrical conductivity at the same filler volume fraction. This is because smaller particles distribute more uniformly throughout the copper matrix, preventing the formation of large insulating clusters and keeping the overall resistivity within a narrow and manageable range [19]. Performance data for typical functional SiC-reinforced composites and films are organized in Table 4.

Table 4. Electrical performance parameters of various SiC-reinforced composites and thin films

Composite / Film System	Composition / Matrix	Key Electrical Metric Range	Primary Transport Modulation Mechanism
Metal-Matrix Composites (MMC)	Cu+SiC (2.5 to 7.5 vol.%)	Conductivity: 58 MS/m down to 46 MS/m	Structural carrier scattering at metal-filler junctions and residual micro-porosity.
Nano-filler Reinforced Matrix	Cu+50 nm SiC particles (10 wt.%)	Resistivity: 3.2 to 4.8 $\mu\Omega\cdot\text{cm}$	Uniform phase distribution suppressing macro-insulating aggregates (15% higher conductivity vs. micro-fillers).
Polymer Nanocomposites	PVA / PS matrix + SiC filler	Dielectric Constant (ϵ'): 5.4 up to 18.2 at 100 Hz	Formation of localized micro-capacitor networks triggering intense interfacial Maxwell-Wagner polarization.
Thin-Film Gas Sensors	Thin-film SiC (50 nm vs. 200 nm)	Response time: Drops from 45 sec down to 12 sec under H ₂	Surface-to-volume scaling ratios; accelerated gas adsorption and rapid surface charge exchange kinetics.
Al-Matrix Composites	Al+SiC (Over-sintered)	Severe spike in net electrical resistivity	Parasitic chemical reactions forming the highly non-conductive aluminum carbide (Al ₄ C ₃) phase.

Dielectric Modulation, Thin-Film Sensors, and Consolidation Effects

In polymer-matrix systems designed for flexible shielding and high-frequency applications, the semi-

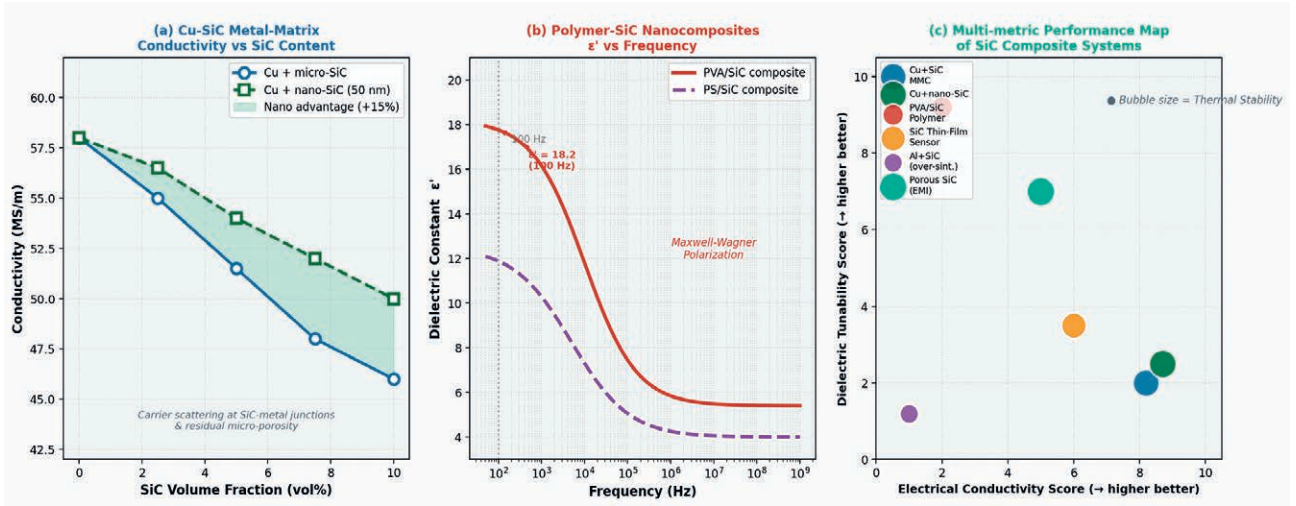


Figure 3. Electrical performance comparison of SiC-based composite systems: (a) Cu-SiC conductivity vs. filler content, (b) dielectric constant vs. frequency for polymer-SiC composites, (c) multi-metric performance map of SiC composite systems

insulating nature of SiC is used directly to tune dielectric properties. When SiC particles are added to polyvinyl alcohol (PVA) or polystyrene (PS) matrices, they create localized micro-capacitor networks that trigger strong interfacial polarization. Through this percolation mechanism, the baseline dielectric constant increases by more than 200%, rising from 5.4 up to 18.2 at 100 Hz, while also helping to map the thermo-kinetic boundaries of the compound [23, 59, 60].

For thin-film sensor applications, electrical transport is controlled primarily by the surface-to-volume ratio of the film rather than its bulk properties. In hydrogen (H_2) sensing films that show a 40% resistance change under 1000 ppm H_2 at 200 °C, reducing the film thickness from 200 nm down to 50 nm cuts the response time from 45 seconds to just 12 seconds. This improvement happens because thinner films allow faster gas adsorption and quicker surface charge exchange [21]. The overall transport efficiency of these composite structures also depends strongly on how the material is consolidated. Spark Plasma Sintering (SPS) produces electrical conductivity about 10% higher than standard powder metallurgy methods, because it creates better bonding between grains and reduces local contact resistance barriers [61].

5. ELECTRONIC TRANSPORT IN LOW-DIMENSIONAL SiC NANOSTRUCTURES

In low-dimensional SiC structures, quantum confinement enables transport behaviors beyond bulk limits. Top-gated nanowire FETs (NW-FETs) deliver an exceptional switching ratio (I_{on}/I_{off}) of $\sim 10^7$ and subthreshold swing of 150 mV/dec at 300 °C – far exceeding planar MOSFETs [20]. Hollow nanotube geometries reduce the field-emission threshold further to 1.8 V/ μm via tip-enhanced local fields [39], though

surface oxygen functionalization can reduce conductivity tenfold by creating trap states [39].

This surface sensitivity becomes an asset in core-shell architectures. A graphitic shell of 2–10 nm grown around a SiC core boosts conductivity ~ 50 -fold, reaching 2.4 S/cm [24]. In heteroepitaxial 3C-SiC nanolayers on silicon, keeping film thickness below 100 nm suppresses defect density and stabilizes electron mobility at 150...200 $cm^2/V \cdot s$ – unachievable in thick bulk films [11]. Confined silicon vacancies (VSi) achieve room-temperature spin-coherence times of ~ 1.1 ms, making them strong candidates for integrated quantum circuits [11, 22].

6. ELECTROMAGNETIC WAVE ABSORPTION AND DIELECTRIC LOSS MECHANISMS

Microwave absorption in SiC materials requires careful permittivity optimization. Moderate resistivity of 10–100 $\Omega \cdot cm$ is essential in porous SiC ceramics: too conductive causes metallic reflection; too resistive allows wave transmission [23]. Under optimized conditions, a 2.1 mm porous SiC layer achieves a reflection loss (RL) of -55.6 dB, corresponding to $> 99.999\%$ absorption efficiency [23].

To enhance dissipation without increasing surface reflection, carbon-shell coating of SiC nanofibers raises the imaginary permittivity (ϵ'') from 1.5 to 5.8, intensifying Maxwell-Wagner polarization loss [24]. Arranging these fibers into periodic nanochains broadens absorption bandwidth to 4.2 GHz in the X-band [62]. Adding just 5 wt% silver nanoparticles raises the real permittivity (ϵ') to 12.8, enabling a 40% reduction in matching thickness while maintaining RL of -42 dB [63]. Aligning SiC nanofibers to match free-space impedance (377Ω) creates an LC-R metamaterial network achieving -62.4 dB reflection loss across the full Ku-band (12.4...18 GHz), outperforming all randomly oriented configurations [16, 17, 24, 26].

7. RADIATION HARDNESS, HIGH-TEMPERATURE STABILITY, AND DEFECT ENGINEERING

Under combined radiation and thermal stress, 4H-SiC significantly outperforms silicon. Where silicon fails under high neutron doses, 4H-SiC's wide bandgap stabilizes the lattice, keeping carrier concentration decay minimal [64]. In JBS diodes, radiation damage appears mainly as increased leakage current and higher forward voltage drop from vacancy-type defects in the drift layer [65]. Thermally, SiC maintains stable nanoampere-range leakage up to 250°C, while silicon junctions fail above 150 °C [42, 64].

Gate-oxide reliability remains a key weakness. At 175°C, 4H-SiC MOSFETs exhibit severe Bias Temperature Instability (BTI), producing threshold voltage (V_{th}) shifts larger than in silicon – evidence of dense near-interface border traps [42]. Controlling minority carrier lifetimes requires suppressing non-radiative recombination at carbon vacancies (VC) [66]. High-temperature annealing deactivates deep-level traps Z1/2 and EH6/7, improving carrier lifetime in bipolar devices [47]. Carbon-cap annealing and SF-KHII ion implantation further suppress stacking fault expansion, pushing PiN diode breakdown voltage beyond 20 kV [41, 51, 67]. Even porous SiC remains structurally stable at 1000 °C through spontaneous self-healing SiO₂ surface layer formation [17].

8. ADVANCED PROCESSING AND CONTACT ENGINEERING

Realizing SiC's power potential requires precise control of contacts and consolidation. A fundamental asymmetry exists: nickel metallization forms low-resistance contacts on n-type SiC readily, but produces high resistivity on p-type SiC due to a large Schottky barrier – requiring high-temperature rapid thermal annealing to form conductive silicide phases [40]. Spark Plasma Sintering (SPS) surpasses conventional hot-pressing by using localized micro-plasma discharges to clean surface oxides and reduce inter-grain resistance [68], with extended milling times further improving phase homogeneity [18]. In aluminum-SiC systems, exceeding the optimal sintering temperature triggers formation of non-conductive Al₄C₃, sharply raising resistivity [19]. At the water level, chemical-mechanical polishing (CMP) to sub-nanometer roughness on 200 mm substrates is essential to prevent field crowding and maximize epitaxial layer breakdown performance [4].

9. MACHINE LEARNING INTEGRATION IN SiC CRYSTAL GROWTH AND DEFECT CHARACTERIZATION

SiC manufacturing is shifting from manual inspection toward data-driven approaches, with machine learning (ML) applied in two complementary ways: downstream defect classification and upstream growth process control.

For post-growth quality control, Shi et al. [36] developed a CNN-based detection system that rapidly and accurately localizes crystallographic defects. However, Taha [35] highlighted a practical limitation: real-world

performance drops when lighting conditions vary, surface backgrounds differ, or training datasets are imbalanced.

On the process control side, Petkovic et al. [37] showed that ML algorithms could replace computationally expensive multi-physics simulations by accurately predicting thermal fields and stress distributions during crystal growth. Azam et al. [38] extended this specifically to SiC, demonstrating real-time defect control during Physical Vapor Transport (PVT) by dynamically modeling temperature gradients and transport kinetics. Together, CNN-based inspection [35, 36] protects wafer quality at the screening stage, while ML-guided process control [37, 38] addresses defect prevention at the source – offering the most direct path to reducing dislocations and stacking faults before they form.

CONCLUSIONS

This review synthesizes cross-scale electronic transport and dielectric loss mechanisms in SiC-based systems, spanning bulk polytypes, porous ceramics, metal-matrix and polymer composites, and low-dimensional nanostructures. The analysis connects fundamental quantum confinement and morphological engineering effects to practical device performance, while documenting the field's industrial maturation toward 200 mm wafer production and renewed interest in 3C-SiC heteroepitaxy for MEMS and quantum applications.

Despite strong intrinsic material properties, several critical challenges continue to limit SiC device performance:

- high interface trap density (D_{it}) at the SiC/SiO₂ boundary reduces inversion-layer channel mobility to just 20...50 cm²/V·s;
- Bias Temperature Instability (BTI) causes threshold voltage shifts under combined thermal and electrical stress;
- p-type Ohmic contact resistance remains unacceptably high for bipolar power devices;
- Lifetime-limiting defects carbon vacancies (VC), deep-level traps (Z1/2, EH6/7), and Shockley stacking faults constrain high-voltage reliability.

Future work should prioritize three directions. First, atomic-level gate dielectric passivation using CO₂, NO, or phosphoryl chloride annealing – to push (D_{it}) below 10¹¹ cm⁻²eV⁻¹. Second, structural defect suppression via high-energy ion implantation (SF-KHII) prior to epitaxial growth. Third, integration of convolutional neural networks for automated wafer defect classification to maximize manufacturing yields. Expanding mesoscale composite engineering in polystyrene-based SiC nanocomposites also offers promising routes toward customizable dielectric and EMI shielding performance in extreme-environment systems.

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ОБЗОР: ЭЛЕКТРИЧЕСКИЕ СВОЙСТВА КОМПОЗИТНЫХ МАТЕРИАЛОВ
НА ОСНОВЕ КАРБИДА КРЕМНИЯ

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Данный обзор посвящён кросс-масштабному анализу электронного транспорта и диэлектрических потерь в системах на основе карбида кремния; также рассмотрены три основные формы кристалла: 4H-SiC, 6H-SiC и 3C-SiC. Лучшим для мощных устройств считается 4H-SiC. Главная проблема – это дефекты на границе SiC и оксида кремния (SiO₂), которые снижают проводимость транзисторов. Также сложно создавать качественные контакты для р-типа и обеспечивать стабильность при длительной работе. На наноуровне SiC используется в квантовых вычислениях и датчиках. В композитах с металлами и полимерами SiC используется для поглощения электромагнитных волн и теплоотвода. Нейросети помогают автоматически выявлять дефекты на пластинах диаметром 200 мм. Главный вывод: будущее SiC-технологий не в улучшении самого кристалла, а в точном контроле его поверхностей и границ.

Ключевые слова: SiC, электрические свойства, широкий запрещённый промежуток, перенос заряда, интерфейсные ловушки, нанокompозиты, омические контакты, силовая электроника, высокотемпературные устройства.

ШОЛУ: КРЕМНИЙ КАРБИДІ (SiC) НЕГІЗІНДЕГІ КОМПОЗИТТІК МАТЕРІАЛДАРДЫҢ
ЭЛЕКТРЛІК ҚАСИЕТТЕРІ

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Бұл шолу кремний карбиді негізіндегі жүйелердегі электрондық тасымал мен диэлектрлік шығындарды әртүрлі масштабтар деңгейінде кешенді талдауға арналған. Сонымен қатар үш негізгі кристалл түрі қарастырылды: 4H-SiC, 6H-SiC және 3C-SiC. Қуатты құрылғылар үшін ең жақсысы 4H-SiC. Басты мәселе SiC пен SiO₂ арасындағы шекарадағы ақаулар, олар транзисторлардың өткізгіштігін төмендетеді. Сонымен қатар р-типті контактілер жасау және ұзақ жұмыс кезіндегі тұрақтылықты қамтамасыз ету қиын болып қалып отыр. Нанодеңгейде SiC кванттық есептеулерде және сенсорларда қолданылады. Металл және полимер композиттерінде электромагниттік толқындарды жұту және жылуды бөлу үшін пайдаланылады. Жасанды нейрондық желілер 200 мм пластиналардағы ақауларды автоматты түрде анықтауға көмектеседі.

Түйін сөздер: SiC, электрлік қасиеттер, кең тыйым салынған аймақ, заряд тасымалы, интерфейс тұзақтары, нанокompозиттер, омикалық контактілер, қуатты электроника, жоғары температуралық құрылғылар.